#2

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Attorney Docket No.: **Poly-22-1/APP**

Applicants: **Eiji OKI et al.**

Serial No.: **09/911,044**

Filing Date: **July 23, 2001**

Title: **SCHEDULING THE DISPATCH OF CELLS IN NON-EMPTY VIRTUAL OUTPUT QUEUES OF MULTISTAGE SWITCHES USING A PIPELINED ARBITRATION SCHEME**

Examiner: **Not yet assigned**

Group Art Unit: **Not yet assigned**

Assistant Commissioner for Patents
Washington, D.C.   20231

S I R:

Information Disclosure Statement

The applicants respectfully request that the references listed on the attached PTO-FORM-1449 be considered in the examination of the above-identified application. A copy of each of these references is enclosed.

The applicants preserve the right to establish that any of the references listed on the attached PTO-FORM-1449 are not prior art to the above-captioned application.
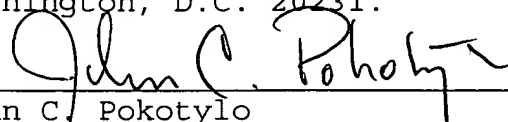
Respectfully submitted,

Dated: August 17, 2001

John C. Pokotylo, Attorney
Reg. No. 36,242
Customer No. 26479
(732) 335-1222

-1-

STRAUB & POKOTYLO
1 Bethany Road
Suite 83, Bldg. 6
Hazlet, New Jersey 07730

CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)

I hereby certify that this correspondence is being deposited on **August 17, 2001** with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

John C. Pokotylo

36,242

Reg. No.

(modified PTO-1449)

U. Department of Commerce
Patent and Trademark Office

LIST OF REFERENCES CITED BY
APPLICANT
(use as many sheets as necessary)

|	
Application Number:	**09/911,044**
Filing Date:	**July 23, 2001**
First Named Inventor:	**Eiji Oki**
Group Art Unit:	**Not yet assigned**
Examiner Name:	**Not yet assigned**
Attorney Docket No.:	**Poly-22-1/APP**

Complete if Known

Sheet	1	of	1

OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, country, where published, source	T[2]
	AA.	N. W. McKeown, "Scheduling Algorithms for Input-Queued Cell Switches," PhD Thesis, University of California at Berkeley, (1995).	
	AB.	C. Y. Lee and A. Y. Oruç, "A Fast Parallel Algorithm for Routing Unicast Assignments in Benes Networks," IEEE Trans. on Parallel and Distributed Sys., Vol. 6, No. 3, pp. 329-334 (March 1995).	
	AC.	T. T. Lee and S-Y Liew, "Parallel Routing Algorithms in Benes-Clos Networks," Proc. IEEE INFOCOM '96, pp. 279-286 (1996).	
	AD.	N. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, "Tiny-Tera: A Packet Switch Core," IEEE Micro., pp. 26-33 (Jan-Feb. 1997).	
	AE.	T. Chaney, J. A. Fingerhut, M. Flucke, J. S. Turner, "Design of a Gigabit ATM Switch," Proc. IEEE INFOCOM '97, pp. 2-11 (April 1997).	
	AF.	F. M. Chiussi, J. G. Kneuer, and V. P. Kumar, "Low-Cost Scalable Switching Solutions for Broadband Networking: The ATLANTA Architecture and Chipset," IEEE Commun. Mag., pp. 44-53 (Dec. 1997).	
	AG.	J. Turner and N. Yamanaka, "Architectural Choices in Large Scale ATM Switches," IEICE Trans. Commun., Vol. E81-B, No. 2, pp. 120-137 (Feb. 1998).	
	AH.	H. J. Chao and J-S Park, "Centralized Contention Resolution Schemes for a Large-Capacity Optical ATM Switch," Proc. IEEE ATM Workshop '97, pp. 11-16 (Fairfax, VA, May 1998).	
	AI.	G. Nong, J. K. Muppala and M. Hamdi, "Analysis of Nonblocking ATM Switches with Multiple Input Queues," IEEE/ACM Transactions on Networking, Vol. 7, No. 1, pp. 60-74 (Feb. 1999).	
	AJ.	N. McKeown, "The iSLIP Scheduling Algorithm for Input-Queued Switches," IEEE/ACM Transactions on Networking, Vol. 7, No. 2, pp. 188-201 (April 1999).	
	AK.	A. Smiljanić, R. Fan and G. Ramamurthy, "RRGS-Round-Robin Greedy Scheduling for Electronic/Optical Terabit Switches," Global Telecommunications Conference – Globecom '99, pp. 1244-1250 (May 1999).	
	AL.	N. McKeown, A. Mekkittikul, V. Anantharam, and J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch," IEEE Trans. on Communications, Vol. 47, No. 8, pp. 1260-1267 (Aug. 1999).	
	AM.	E. Oki, N. Yamanaka, Y. Ohtomo, K. Okazaki and R. Kawano, "A 10-Gb/s (1.25 Gb/s x 8) 4 x 2 0.25-μm CMOS/SIMOX ATM Switch Based on Scalable Distributed Arbitration," IEEE J. of Solid-State Circuits, Vol. 34, No. 12, pp. 1921-1934 (Dec. 1999).	
	AN.	N. Yamanaka, E. Oki, S. Yasukawa, R. Kawano and K. Okazaki, "OPTIMA: Scalable, Multi-Stage, 640-Gbit/s ATM Switching System Based on Advanced Electronic and Optical WDM Technologies," IEICE Trans. Commun., Vol. E83-B, No. 7, pp. 1488-1496 (July 2000).	
	AO.	J. Chao, "Saturn: A Terabit Packet Switch Using Dual Round-Robin," IEEE Communications Magazine, pp. 78-84 (Dec. 2000).	
	AP.	G. Nong and M. Hamdi, "On the Provision of Quality-of-Service Guarantees for Input	
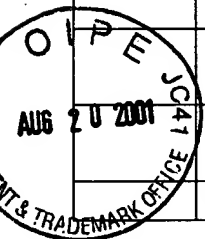
		Queued Switches," IEEE Commun. Mag., pp. 62-69 (Dec. 2000).	
AQ.		E. Oki, Z. Jing, R. Rojas-Cessa, J. Chao, "Concurrent Round-Robin Dispatching Scheme in a Clos-Network Switch," IEEE ICC 2001, pp. 106-112 (June 2001).	
AR.		E. Oki, R. Rojas-Cessa and H. J. Chao, "PCRRD: A Pipeline-Based Concurrent Round-Robin Dispatching Scheme for Clos-Network Switches," pp. 1-18.	
AS.		A. Smiljanić, "Flexible Bandwidth Allocation in Terabit Packet Switches," pp. 233-239.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Unique citation designation number. 2 Applicant is to place a check mark here if English language translation is attached.